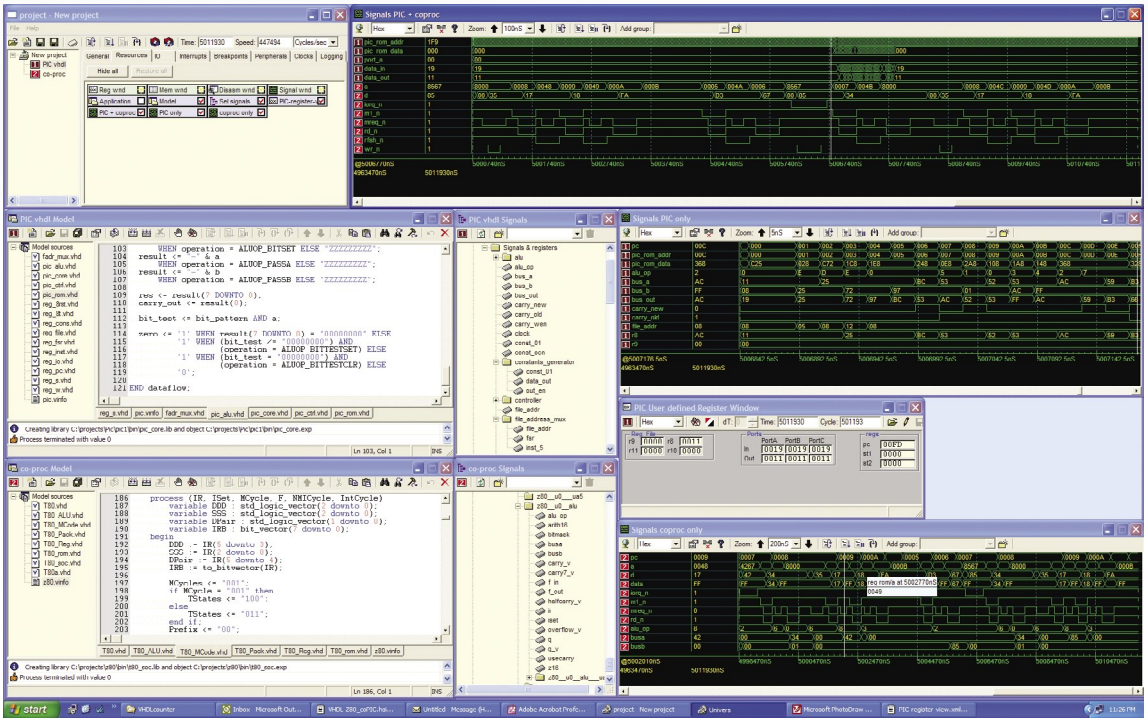
UNIVERS RTSIM

Astonishing high RTL simulation speed!

GENERAL DESCRIPTION

Univers® RTSIM is a stand-alone simulation environment dedicated to the Register Transfer Level of hardware description languages. It's one of the fastest hardware verification tools, available on a computer and includes an editor, waveform viewer and other advanced debugging tools. A simulation speed increase of a factor 10x to 100x is possible.Univers RTSIM is the Integrated System RTL Simulation tool of Adveda's UNIfied VERification Solutions.



Univers RTSIM is a stand-alone simulator, which offers the Hardware Engineer one central cockpit from which he can perform all his code editing and code verification. Univers RTSIM is one of the fastest available cycle-based RTL simulators. Here is a short summary of the main features:

- Ultra fast Native Compiled Verilog/VHDL simulation
- Cycle-based technology and 2-state logic models
- Complete IDE with editor
- Open debug-API for integration
- Extensive and unique debug features
- Graphical static and dynamic profiling
- Integrated stimuli signal generator
- Full featured Memory Windows for RTL-coded memories
- On-Screen data coloring to improve visibility

UNIVERS FAMILY

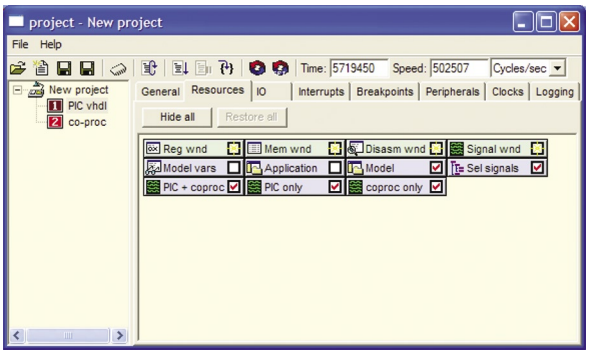
Meet the family

Univers RTSIM is part of Adveda's Univers family. Univers ISSIM is a standalone software development and debug environment, with the same graphical user interface and Univers COVER is the combination of Univers ISSIM and Univers RTSIM and delivers a complete system-level cycle-accurate simulation of both hardware and software at an unsurpassed speed.

Central to all debug sessions with Univers RTSIM are the Project Window and the RTL Model Window, which represents the application in RTL source code. Memories can be either modeled in RTL or within the Univers concept. Both types can be viewed in the dedicated Memory Windows. All signals can be viewed in a Waveform Window. A customizable register view can be built for ease of debugging. All usual run-control functions are provided through menus and icon-buttons within the context of different windows. All settings of the project are saved in a XML-formatted project file.

PROJECT WINDOW

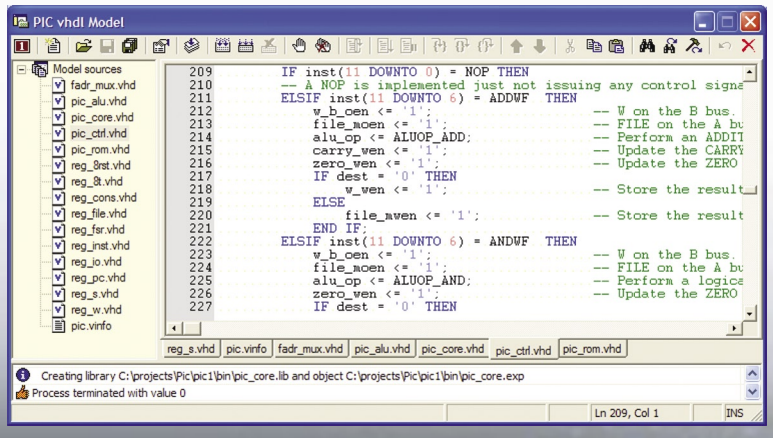
The Project Window instantiates the project and controls the overall debug process. At the top level every RTL module has its own list of features and relevant debugging windows. All these windows can be managed from the Project Window.
The Project Window also contains a logging field as well as a command prompt. Furthermore, external clocks, IO, DMA, breakpoint settings as well as inter-processing communication can be setup via this window.

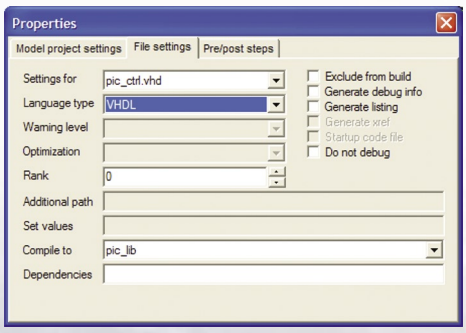


RTL MODEL WINDOW

Every RTL module has a Model Window, which contains the RTL source codes of such a module. Within the Model Window, the RTL code can be viewed, edited and (re-) compiled. The RTL code is context-sensitively colored for ease of reading.

For easy debugging, the values of signals pop-up when the mouse is moved over the associated source code text. Breakpoints in your RTL code can be placed as well.





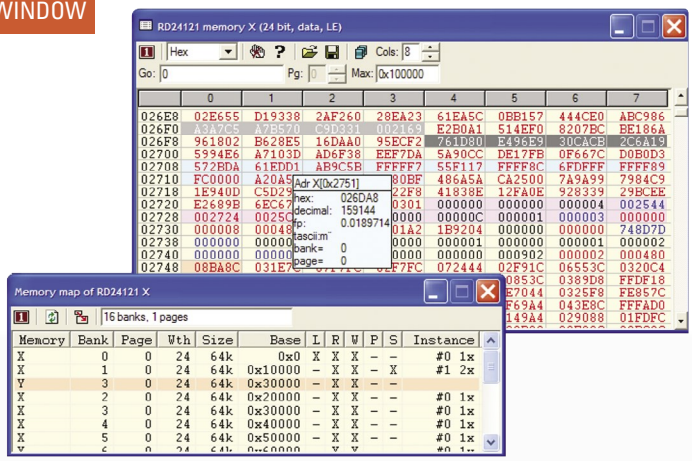
RTL simulation at unsurpassed speed

THE SPEED

Univers RTSIM is using several novel approaches to reach the maximum possible speed for an RTL simulator. It is not targeted to gate-level simulation and solely optimized for speed at the Register Transfer Level. It is using a cycle-based approach to reach the ultimate speed, while still handling any number of asynchronous clocks. Furthermore, after checking your initial reset conditions, the 9-state (VHDL) and 4-state (verilog) models are not really useful anymore for most parts of the design and are slowing down the simulator. Univers RTSIM does use a 2-state logic model, where applicable. It can still handle tri-state signals and detect reads from undefined memory locations or from external signals. It supports the full synthesizable RTL Verilog/VHDL syntax.

Univers RTSIM has been benchmarked against traditional event-driven simulators, where it reached two orders of magnitude speed increase.

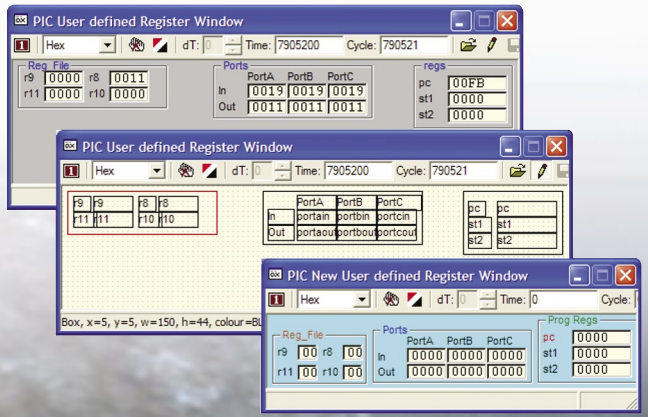
MEMORY WINDOW



Every memory space may be made visible in multiple windows. A memory space may consist of multiple different memory instances and such an instance may again be shared with other memory spaces. Memory spaces may be accessed from multiple RTL modules or external peripherals. When such a memory space is defined within the Univers concept, all types of breakpoints may be set at every individual location or at a range of locations. Furthermore, it enables detailed profiling of memory usage.

REGISTER WINDOW

Software engineers are used to work with register views of their processors. Within Univers RTSIM, users can define their own 'register view', in which they may place any register or signal from the RTL code. Besides just viewing the content of registers, it is possible to overwrite these or set various types of breakpoints for each register. The view of this window may be fully customized by the user.

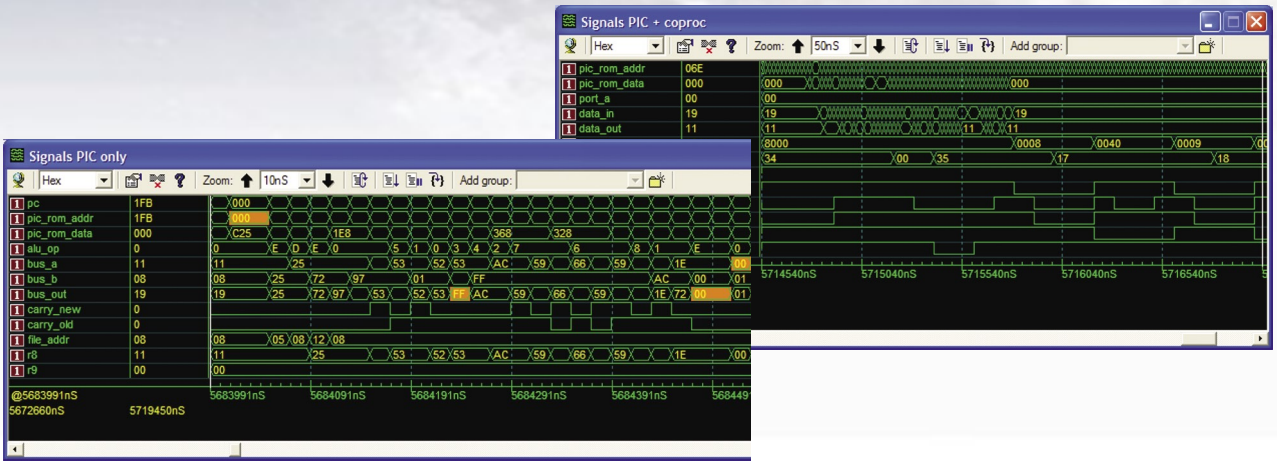


UNIVERS RTSIM

UNIVERS RTSIM

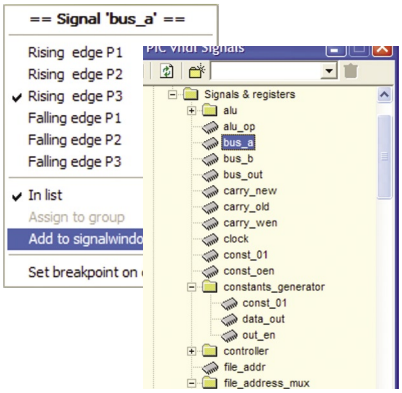
WAVEFORM WINDOW

Within the Waveform Window every signal of the RTL code may be viewed. Also any value from a testbench written in 'C' may be traced in the same Waveform Window. It is possible to have multiple independent Waveform Windows. The window provides multiple additional features like zooming or setting breakpoints on signals. Busses can be color-coded when they are within a certain range of values, thus enabling the quick identification of certain conditions.



SIGNAL WINDOW

All signals of the RTL code are displayed in the Signals Window and can be dragged and dropped from the window into the one of the Waveform Windows. Signals may also be displayed in another window, which gives an overview of the size and the current value of signals.



CONCLUSION

Univers RTSIM uses novel methodologies to reach maximum RTL simulation speed, without sacrificing debugging capabilities. This allows users to simulate more in less in time, resulting in higher first-time right success rates and a shorter time to market.

ADVEDA

VERIFICATION SOLUTIONS FOR CHIP DESIGN

ADVEDA B.V. • FINISTÈRELAAN 18 • 5627 TD EINDHOVEN • THE NETHERLANDS • TEL: +31 40 291 23 85 • FAX: +31 40 291 23 86 • WWW.ADVEDA.COM • INFO@ADVEDA.COM